SRI VENKATESWARA COLLEGE OF ENGINEERING

(AUTONOMOUS)

Karakambadi Road, Tirupati-517507

EXAMINATION BRANCH

R24

M.Tech II Semester (R24) Supplementary Exams October-2025

TIME TABLE

Exam Timings: **9.30 AM TO 12.30 PM**

Date/Day	VLSI Design (VLSI D)	Computer Science and Engineering (CSE)
06-10-2025 (Monday)	CMOS Mixed Signal Design (EC24DPC201)	Advanced Computer Networks (CS24DPC201)
08-10-2025 (Wednesday)	Physical Design Automation (EC24DPC202)	Internet of Things (CS24DPC202)
10-10-2025 (Friday)	MEMS System Design (EC24DPE201)	Deep Learning (CS24DPE201)
14-10-2025 (Tuesday)	Biomedical CMOS IC's (EC24DPE204)	Distributed Systems (CS24DPE205)

Note: Any discrepancy in this time table may be brought to the notice of the under signed immediately.

Controller of Examinations **Dy Chief Superintendent** **Principal**

Date: 22-09-2025